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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/811,666	03/20/2001	Ki-Whan Song	SEC.807	9403
20987	7590	02/15/2005	EXAMINER	
VOLENTINE FRANCO, & WHITT PLLC ONE FREEDOM SQUARE 11951 FREEDOM DRIVE SUITE 1260 RESTON, VA 20190			PAREKH, NITIN	
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			2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No. 09/811,666	Applicant(s) SONG, KI-WHAN	
Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 03 December 2004.  
 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.  
 4a) Of the above claim(s) 5-10 is/are withdrawn from consideration.  
 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
 6) ☒ Claim(s) 1-4 and 11-15 is/are rejected.  
 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☒ The drawing(s) filed on 20 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) in which the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) ☒ All b) ☐ Some \* c) ☐ None of:  
 1. ☒ Certified copies of the priority documents have been received.  
 2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4, 11, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Masakuni et al. (Japanese Pat. 10-284678) and Shimizu et al. (US Pat. 6211576).

Regarding claim 1, the APA discloses a ball grid array (BGA) package/chip scale package (CSP) semiconductor device with two or more external powers including a first and second power, the device comprising:

- a semiconductor chip (120 in Fig. 1A/1B) having a plurality of pads (122 in Fig. 1A/1B) including power and ground pads being arranged along a center of a first surface
- a substrate having a first surface which confronts the first surface of the chip and an opposite second surface, the substrate further having a slot (112 in Fig. 1A/1B) extending there through which is aligned over the pads to expose the pads

- a signal line plane (SLP) extending over a two-dimensional area of the second surface of the substrate on two sides of the slot (see signal line pattern 114 in Fig. 1A and the same on the plane/second surface in Fig. 2) including a plurality of wirings/signal line patterns (114 in Fig. 1A) connecting a plurality of power, ground and signal balls mounted on the respective ball mounts (150 and 116 respectively in Fig. 1A) to be connected to an external circuit on its one side and the respective pads of the chip being mounted on the other side through the slot
- a bonding material (140 in Fig. 1B) being inserted between the respective first surfaces of the chip and the substrate to fix the chip to the substrate, and
- a first, second or more than two power supply being applied to the respective one of the plurality of balls in the signal line plane

(Fig. 1A, 1B and 2; specification pages 1-3).

The APA fails to specify:

- the SLP being divided into a first and second SLP over two-dimensional areas on respective side of the slot, each SLP having a rectangular surface area and the first and second planes having a first and second plurality of ball mounts in respective areas where some of the plurality of balls are electrically connected to the respective SLP and others are electrically isolated from the same, and
- a first and second power is applied to at least one of the balls electrically connected to the respective first and second signal line planes respectively.

Masakuni et al. teach using a substrate having a variety of power/signal/ground routing configurations comprising a signal plane in a rectangular/two-dimensional configuration (5c in Drawing 2, 14-18, 1-18; English translation- sec. 0040) where the SLP is divided into two planes having two-dimensional areas including a first and second planes (5c-1 and 5c-2 in Drawing 2, 14-18, etc.) located on a first and second portions of the substrate surface where each portion is on opposing sides of the slot (5C-1 and 5C-2 in Drawing 2, 14, etc.) to provide a design flexibility and optimization for power and ground electrodes and respective routing. Masakuni et al. further teach each planes having any desired level/combination of power/positive voltage or ground potentials to electrically connect the respective power/ground lands/pads and lead wiring (5a and 5d respectively in Drawing 2) to external electrodes/bumps so that the first plane/combined plane/single electrical node has only a first power or ground lines and a second plane/combined plane/single electrical node has only a second power or ground lines (English translation- sec. 0018-0020, 0036-0041, 0066-0070; Drawings 1-17).

Furthermore, such wiring planes/patterns in Masakuni et al. comprise portions having a rectangular shape patterns/areas (see 5c in Fig. 12, 14, 16, etc.).

Shimizu et al. teach a device having a variety of power/ground wiring configurations including the configurations where the ground plane and power plane have surface areas having a conventional rectangular shape (see 1003b in Fig. 7, Col. 9/10 and 2000 in Fig. 19 respectively, Col. 1 respectively).

APA further teaches the conventional configuration having a plurality of signal, power and ground balls/mounts being formed over two dimensional area in a mixed pattern such that some of the plurality of balls/mounts (170 in Fig. 2) within a signal plane are being separated/electrically isolated from the other signal balls/mounts (Fig. 1A/B and 2; specification pages 1-3).

Furthermore, selection and determination of parameters such as number/spacing of ball/mount/pad connections, number of power/ground/signal layers, a shape/layout/pattern of such connections in each layer, etc. in chip scale packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired noise/cross-talk reduction, grounding and signal distribution for the device.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the SLP being divided into a first and second planes over two-dimensional areas on respective side of the slot, each SLP having a rectangular surface area the first and second planes having a first and second plurality of ball mounts in respective areas where some of the plurality of balls are electrically connected to the respective signal line plane and others are electrically isolated from the same and a first and second power being applied to at least one of the balls electrically connected to the respective first and second signal line planes respectively

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as taught by Masakuni et al. and Shimizu et al. so that the routing for the power and ground electrodes can be optimized and electrical performance and external connection flexibility can be improved in APA's BGA.

Regarding claim 2, APA, Masakuni et al. and Shimizu et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Masakuni et al. teach the first and second power lines forming the combined first and second planes respectively exhibiting a single node electrically (Masakuni et al.: English translation- sec. 0018-0020, 0036-0041, 0066-0070; Drawings 2 and 14).

Regarding claim 3, APA, Masakuni et al. and Shimizu et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein the APA teaches the device being a chip scale package.

Regarding claim 4, APA, Masakuni et al. and Shimizu et al. teach substantially the entire claimed structure as applied to claim 1 above, including the first power being a positive voltage and the second power being a ground (Masakuni et al.: English translation- sec. 0018-0020, 0036-0041, 0066-0070; Drawings 2 and 14).

Regarding claim 11, APA, Masakuni et al. and Shimizu et al. teach substantially the entire claimed structure as applied to claim 1 above including the power and ground

planes being over the first and second surface areas/two dimensional areas respectively, except a plurality of signal balls mounts being located within and electrically isolated from at least one of the first and second two-dimensional areas having power and ground planes respectively.

APA further teaches the conventional electrode pad/wiring configuration having a plurality of signal, power and ground balls/mounts being formed in the two dimensional area in a mixed pattern such that some of the plurality of balls/mounts (170 in Fig. 2) within the signal plane are being separated/electrically isolated from the other power and ground balls/mounts (Fig. 1A/B and 2; specification pages 1-3).

Furthermore, selection and determination of parameters such as number/spacing of ball/mount/pad connections, number of power/ground/signal layers, a shape/layout/pattern of such connections in each layer, etc. in chip scale packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired noise/cross-talk reduction, grounding and signal distribution for the device.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate power and ground planes being over first and second two-dimensional areas respectively and a plurality of signal balls mounts being located within and electrically isolated from at least one of the first and second two-dimensional areas having power and ground planes respectively so that the routing for



the power and ground electrodes can be optimized and electrical performance and external connection flexibility can be improved in Masakuni et al. and APA's BGA.

Regarding claim 14, APA, Masakuni et al. and Shimizu et al. teach substantially the entire claimed structure as applied to claim 11 above, wherein the APA further teaches using the conventional layout having two or more external power supplies/external circuits where the power or ground balls/mounts are formed on both sides of the slot in a mixed pattern and are being separated from the respective planes (Fig. 1A/B and 2; specification pages 1-3).

Regarding claim 15, APA, Masakuni et al. and Shimizu et al. teach substantially the entire claimed structure as applied to claim 11 above, wherein the APA further teaches using the conventional layout having two or more external circuits where the power or ground balls/mounts are formed on both sides of the slot in a mixed pattern and are being separated from the respective planes (Fig. 1A/B and 2; specification pages 1-3).

5. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA), Masakuni et al. (Japanese Pat. 10-284678) and Shimizu et al. (US Pat. 6211576) as applied to claim 11 above, and further in view of Stearns et al. (US Pat. 5895967) and Kirkman (US Pat. 6064113).

Regarding claim 12, APA, Masakuni et al. Shimizu et al. teach substantially the entire claimed structure as applied to claim 11 above, except a boundary defining the power plane wrapping around signal ball mounts positioned on the power plane and their interconnection lines.

Stearns et al. and Kirkman teach using conventional routing layout/design where the power and ground planes wrap around power, ground or signal ball mounts and interconnection lines at any desired level in the substrate (Stearns et al - Fig. 3; Col. 5 and 6; Kirkman- Fig. 4 and 5; Col. 7 and 8) to achieve the optimized routing and electrical performance.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the boundary defining the power plane wrapping around signal ball mounts positioned on the power plane and their interconnection lines as taught by Stearns et al. and Kirkman so that the routing for the power and ground electrodes can be optimized to improve the electrical performance in Shimizu et al., Masakuni et al. and APA's BGA.

Regarding claim 13, APA, Masakuni et al. Shimizu et al. teach substantially the entire claimed structure as applied to claim 11 above, except a boundary defining the ground plane wrapping around signal ball mounts positioned on the ground plane and their interconnection lines.

Stearns et al. and Kirkman teach using conventional routing layout/design where the power and ground planes wrap around power, ground or signal ball mounts and interconnection lines at any desired level in the substrate (Stearns et al - Fig. 3; Col. 5 and 6; Kirkman- Fig. 4 and 5; Col. 7 and 8) to achieve the optimized routing and electrical performance.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the boundary defining the ground plane wrapping around signal ball mounts positioned on the ground plane and their interconnection lines as taught by Stearns et al. and Kirkman so that the routing for the power and ground electrodes can be optimized to improve the electrical performance in Shimizu et al., Masakuni et al. and APA's BGA.

### ***Response to Arguments***

6. Applicant's arguments filed on 12-03-04 have been fully considered but they are not persuasive.

A. Applicant contends that Masakuni et al. disclose the tape carrier package (TCP) having the flexible tape substrate and one of ordinary skill in the art would not be motivated to combine Masakuni et al's electrodes with the APA.

However, as explained above, Masakuni et al. teach the TCP having the substrate as recited in the independent claims. Such power/ground wiring structure

having external electrodes is conventionally used in BGA packages comprising a variety of substrates having rigid or flexible properties.

B. Applicant contends that Masakuni et al's balls are vertically offset and do not rest on the common wiring as those in the APA, therefore the combination of Masakuni et al. with the APA is not proper.

However, the balls in Masakuni et al. are electrically connected with respective mounting lands/pads on the respective wiring plane as claimed. Therefore, Masakuni et al's power/ground wiring and electrode configuration is applied to the APA.

### ***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

02-12-05



NITIN PAREKH

PATENT EXAMINER

TECHNOLOGY CENTER 2800